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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

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1 of 1

Complete if Known

Application Number	
Filing Date	June 28, 2003
First Named Inventor	Chih-Hsin Wang
Art Unit	
Examiner Name	

Attorney Docket Number

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
CH		US- 5,780,341	07-14-1998	Seiki Ogura	Figs.4A,4B,6A,6B
		US-			Fig. 7A
MH		US- 4,957,877	09-18-1990	Simon M. Tam et al.	Figs. 5A, 5B
MH		US- 5,146,426	09-08-1992	Mukherjee , et al	p2, c5 L17-20
		US-			c3 L46-48, c6 L45-53
MH		US- 5,432,739	07-11-1995	H. B. Pein	c3 L57-65
		US-			
MH		US- 5,115,289	05-19-1992	Hisamoto et al.	Figs.1,3b
		US-			c10 L66-68, c11 L44
		US-			c13 L27, c17 L14-68
MH		US- 6,479,863 B2	11-12-2002	John Caywood	Figs. 3b, 5b, 17d,
		US-			17e,18d
MH		US- 6,372,617 B1	04-16-2002	T. Kitamura	Fig. 3A
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶

Examiner
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04/23/04

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Sheet	1	of	1	Attorney Docket Number
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
CHK		Kitamura et al., "A Low Voltage Operating Flash Cell with High Coupling Ratio Using Horned Floating Gate with Fine HSG," <i>Symposium on VLSI Technology</i> , p.104, 1998	
CHK		Lai, "Flash Memories: Where We Were and Where We Are Going", <i>IEDM Technical Digest</i> , pp.971-973, 1998	
CHK		Kuo et al., "TEFET - A High Density, Low Erase Voltage, Trench Flash EEPROM", <i>Symposium on VLSI Technology</i> , p.51, 1994	
CHK		Wang et al, "Three-Dimensional DIBL for Shallow-Trench Isolated MOSFET's", <i>IEEE Trans. on Electron Devices</i> , vol. 46, pp. 139-144, 1999	

Examiner Signature	<i>Chih-Hsin Wang</i>	Date Considered	04/23/04
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